Embedded Device Packaging
Ramping Up Next Generation SiP

JISSO European Council Seminar, Nürnberg
May 2011
Race to the “perfect” device ...

Tablets of the past

Space is a commodity we must strive (and design) to use less of ...

\[ \text{mm}^3 = \text{cost}, \text{mm}^3 = \text{efficiency}, \text{mm}^3 = \text{competitiveness} \]
Hopefully over the next 15 minutes I can give an introduction to ...

- Pre-cursors
- ECP® - AT&S chip embedding technology
- The integration challenge - Smartphone >>> Industrial >>> Automotive
- Competitive picture
- Application examples
- Process flow and fab overview
- Roadmap and Ecosystem for embedded die ...
- Wrapping up
A new standard ...

Package Types (common)

- QFN – Quad Flat No-lead
- QFP – Quad Flat Pack
- IPD – Integrated Passive Device
- SIP – System in Package
- SIB – System in Board
- MCM – Multi Chip Module
- PGA - Pin grid array
- LGA - Land grid array
- DIP – Dual Inline Package
- SOIC – Small Outline Integrated Circuit
- BGA – Ball Grid Array
- LTCC – Low Temperature Co-fired Ceramic
- **ECP® - Embedded Component Package**
Statements

- Mass production PCB technology is already at stacked microvia, every layer interconnect

- 01005 SMD discretes already in mainstream production

- 0.4mm BGA is standard in all smartphone applications, and cascading into other segments

- The drive is to take more steps, and big steps – thickness reduction, form factor reduction, no reliability compromise
Main ideas ...

- **Reduction**
  - Roadmaps, Roadmaps, Roadmaps – PCB; IC Substrate; Semiconductor ...
  - ... but ... diminishing returns
  - Salami-slicer miniaturisation ...

- **Elimination**
  - When was the last time a feature was eliminated? More like added ...
  - Adding to the challenge

- **Combination**
  - Surely this will yield the most major benefits ...
We believe the next step...
Competitive Landscape ... “the train is running”

- Two emerging technologies
- Embedded die in laminate (ECP-like) and Fan Out Wafer Level Package (semiconductor basis)

Source: Yole Developpement
Take a simple DC-DC convertor

Solder-ball or copper pad for PCB attach
Embedded active component
Surface mount components
Typically two redistribution layers

Package layout
- High performance DC-DC Convertor for smartphone application
- Package 2.3mm x 2.9mm x 1mm (x-y-z)
- Integrated solution
- Sourcing one component instead of four
Next generation DC-DC SiP using ECP®

- For the same current-handling capability...
- ... a footprint reduction of **FACTOR 12** ... over the last 10 years
- Further twofold reduction utilising ECP® compared to conventional package ...
- ... with more possible (50% again)
- All ECP® SiPs under 1mm total assembled thickness
Specialist Packaging for Reliability – Automotive

Intelligent Power Modules

Heat Dissipation, Reliability & Size driven

MEMS & Sensor Modules

Reliability, Size & Cost driven

Engine Control Module

ECP® Automotive

Reliability, Redistribution & Size driven

Telematics/Infotainment

High Performance opportunities

Source: Yole Developpement

Advanced Packaging

AdvancedPackaging

www.ats.net
Bosch Engine Control Module - HERMES

Design rule 25μm line
6-layer package
Medical Packaging - WL-CSP on Rigid-Flex

1000 hrs HTOL @ 125°C, 100mA passed
1000 hrs High Temp @ 150°C passed
Autoclave 121°C, 2atm, 168 hr passed
Temp. Humidity Bias (1000hrs 85/85 RH) passed
AATC 1000 cycles (-55°C/+125°C) passed
Mechanical Shock (1500G, 0.5ms, 6 axis) passed
Centrifuge (10,000G) passed

Chip-Set for Pacemaker
Digital Circuitry: 33 I/Os
IRA: 29 I/Os
Analog Circuitry: 9 I/Os
Mixed Signal ASIC: 120 I/Os

Source: Fraunhofer IZM
## ECP® Technology - Application Areas

<table>
<thead>
<tr>
<th>Definition</th>
<th>Printed Wiring Board with Embedded Component – System in Board</th>
<th>Integrated Component Packaging – Single Chip and System in Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECP® releases surface space for other components or allows the overall PWB size to be reduced</td>
<td>ECP® allows packaging of single chips and highly integrated modules. Flexibility to incorporate different device technologies within one component</td>
<td></td>
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### Applications

<table>
<thead>
<tr>
<th>Printed Wiring Board</th>
<th>Integrated Component Packaging – Single Chip and System in Package</th>
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<tbody>
<tr>
<td>Mobile phone engine board</td>
<td>Single Chip Packaging (Fan-out)</td>
</tr>
<tr>
<td>Portable devices</td>
<td>ESD/EMI protection networks</td>
</tr>
<tr>
<td>Industrial main board</td>
<td>Power MosFet</td>
</tr>
<tr>
<td>Medical applications</td>
<td>DC/DC converters</td>
</tr>
<tr>
<td>Automotive main board</td>
<td>IC Drivers: Audio Codec, LED driver, display interface, ..</td>
</tr>
<tr>
<td></td>
<td>Transceivers</td>
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</tbody>
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### Benefits

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<th>Printed Wiring Board</th>
<th>Integrated Component Packaging – Single Chip and System in Package</th>
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<tbody>
<tr>
<td>Miniaturization</td>
<td>Miniaturization: Footprint and Low Thickness</td>
</tr>
<tr>
<td>Improved electrical performance</td>
<td>Improved electrical and thermal performance</td>
</tr>
<tr>
<td>Improved reliability and mechanical stability</td>
<td>Improved reliability and stability, backside protection</td>
</tr>
<tr>
<td>Improved thermal performance</td>
<td>Design flexibility: 3D routing from front to back of IC</td>
</tr>
<tr>
<td></td>
<td>3D stacking: in package and of packaged ICs</td>
</tr>
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<td>Lower cost potential</td>
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BLAP Virtual Tour

AT&S Advanced Packaging Fab

- Clean room Class 10,000 1,200 m²
- Clean room Class 1,000 200 m²
- General Manufacturing 1,000 m²

Capacity ca. 20M single chip packages per month

Investment so far (equipment) ca. 15M USD
Process flow

1. Component Supply
2. Laser-Drilling of fiducials + overlay
3. Printing of Adhesive
4. Vacuum treatment of Adhesive
5. Assembly of Components
6. Curing of Adhesive
7. Lay up & Pressing
8. Mechanical-Drilling
9. UV Laser Drilling
10. CO2 Laser Desmear
11. E-less Copper
12. Imaging
13. Developing
14. Copper plating
15. Stripping/Etching
16. 100% Automatic Optical Inspection
17. Solder mask
18. Routing
19. Electrical test
20. OSP
21. Final Inspection
22. Module Supplier

Advanced Packaging
ECP Area 1: Assembly, Inspection, Final testing

- ECP Area 1 (Cleanroom class 10.000):
  - Printing of adhesive – Assembly of components
  - Optical Inspection (AOI, AOR, Verification)
  - Electrical testing
  - Final Inspection
Assembly of Components

- Assembly of components
  - Machine capability for placement of 2x2 mm ceramic components
  - 20 nozzle Head
    - max. speed: 20000 comp./h
    - Accuracy specified: ± 55 μm, ± 0.7° (4σ)
  - Twin Head
    - Max. speed: 3700 comp./h
    - Accuracy specified: ± 30 μm, ± 0.07° (4σ)

20 nozzle head  Assembly equipment  Wafer system
Semi Additive Technology

- Developer and resist strip/etch lines with touch-less transport system
- Focus on yield and process capability
- State of the art copper plating
ECP® - Application Roadmap

- Embedded Die
- Embedded Discrete - EDC
- WLP - SiP
- MEMS Packaging
- Embedded PoP
- Embedded SiP Module

Package:
- 2010
- 2011
- 2012
- 2013

- Simple devices in 2/4 layer package, single stack die, 50µm line
- Embedded Passives in Main Board – mainly discrete and simple integrated devices
- 1-2 chip in package combined with surface mount, single stack 35µm line
- MEMS package using AT&S 2.5D technology – microphone, loudspeaker, etc
- High end packaged die for ultra low profile PoP, 25µm line
- Multi-chip, combining discrete devices, Digital and RF, multi-stack, < 25µm line
**Ecosystem**

- EDA software supporting embedded die package design
  - Cadence Allegro 16.5 (supporting ECP®) released this month, currently in Beta
- Major initiative in marketing and dissemination
  - 2 papers delivered at IPC Apex April 2011
  - Papers lined up for Semicon West and Semicon Europe
  - SMT-EIPC workshop of course ...
- HERMES initiative running to a successful conclusion – initial foray to standardise supply chain
- Key supply chain partners identified and committing to roadmaps
- Significant activity in the semiconductor industry – new solutions required and emerging
- Competition in Asia – but this is also good for us!
Wrapping up ...

- Embedded die (laminate technology) is ramping now – the NEED to miniaturise is overwhelming the LIMITS of the supply chain
- First concepts are simple System in Package (SiP), with stacked SiP already in pre-series evaluation
- First commercial products running in series production ramp quantities (up to 5M per month)
- Smartphone is early driver but other applications – automotive and medical – now in prototyping phase
- Embedded device technology is AT&S’s biggest new technology investment – targetting a leadership position ...
AT&S – a Global Electronics Company

- Procurement & Sales: Office in Hong Kong
- Design Capacities: Austria and Germany
- 16 Sales Offices worldwide

ECP® - The Leading Chip Embedding Technology

Thanks for your attention, any questions?