

AT&S Results Q1-3 2025/26

Conference Call

February 3, 2026

The background of the slide is a glowing blue circuit board with intricate patterns of light and lines. In the center, there is a dark blue rectangular box containing the white text "AT&S".

AT&S

Key developments

€ 1.3 BN Revenue

PY: € 1.2 BN

€ 297 MM EBITDA

Margin: 23 %

PY: € 232 MM

€ 34 MM EBIT

Margin: 3 %

PY: € -1 MM

€ 223 MM Operating Free Cash Flow

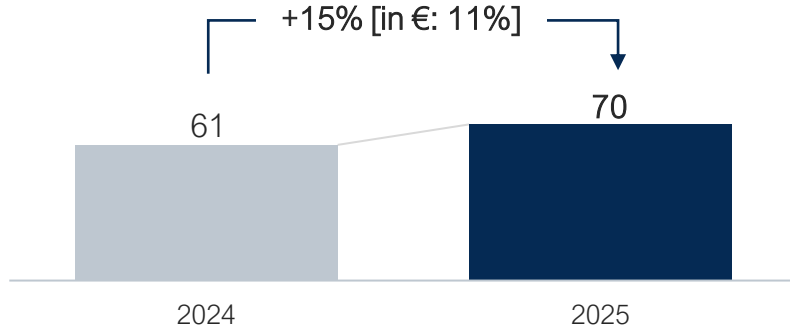
PY: € -357 MM

- As announced: **Kulim and Hinterberg** start contributing to revenue
- Product mix, efficiency programs and improved pricing environment drive **EBIT** development
- Headwinds from **FX effects**
- Global dynamics remain uncertain, but **market environment** becomes more positive
- **Guidance** confirmed

Market stabilizing, visibility remains low

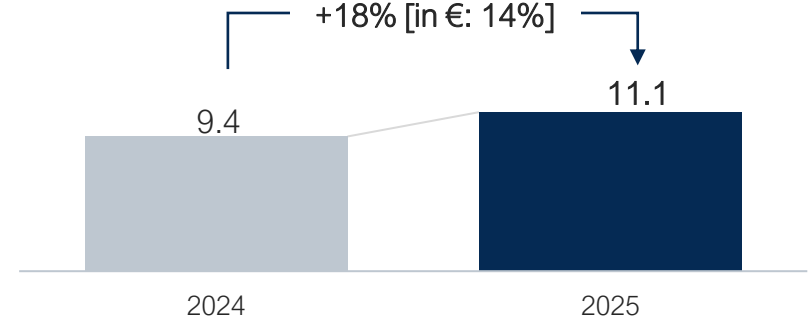
Market development printed circuit boards

in US\$ BN



Market development IC substrates

in US\$ BN



- Markets stable overall, caution persists across Automotive and Industrial due to uncertain geopolitical climate.
- Continued momentum from data center computing due to AI investment.
- Client computing could face headwinds caused by high memory prices, tariffs.

Source: Prismark, January 2026

Management Board

New management structure enabling swift decision-making processes



Dr.-Ing. Michael Mertin
CEO

Responsible for:

- Business Unit Electronics Solutions
- Business Uni Microelectronics
- Communications
- Human Resources
- Legal & Compliance
- Public Affairs
- Strategy & Transformation



Gerrit Steen
CFO

Responsible for:

- Audit
- Controlling
- Finance
- Information Technology
- Investor Relations
- Procurement
- Risk & Continuity Management
- Treasury



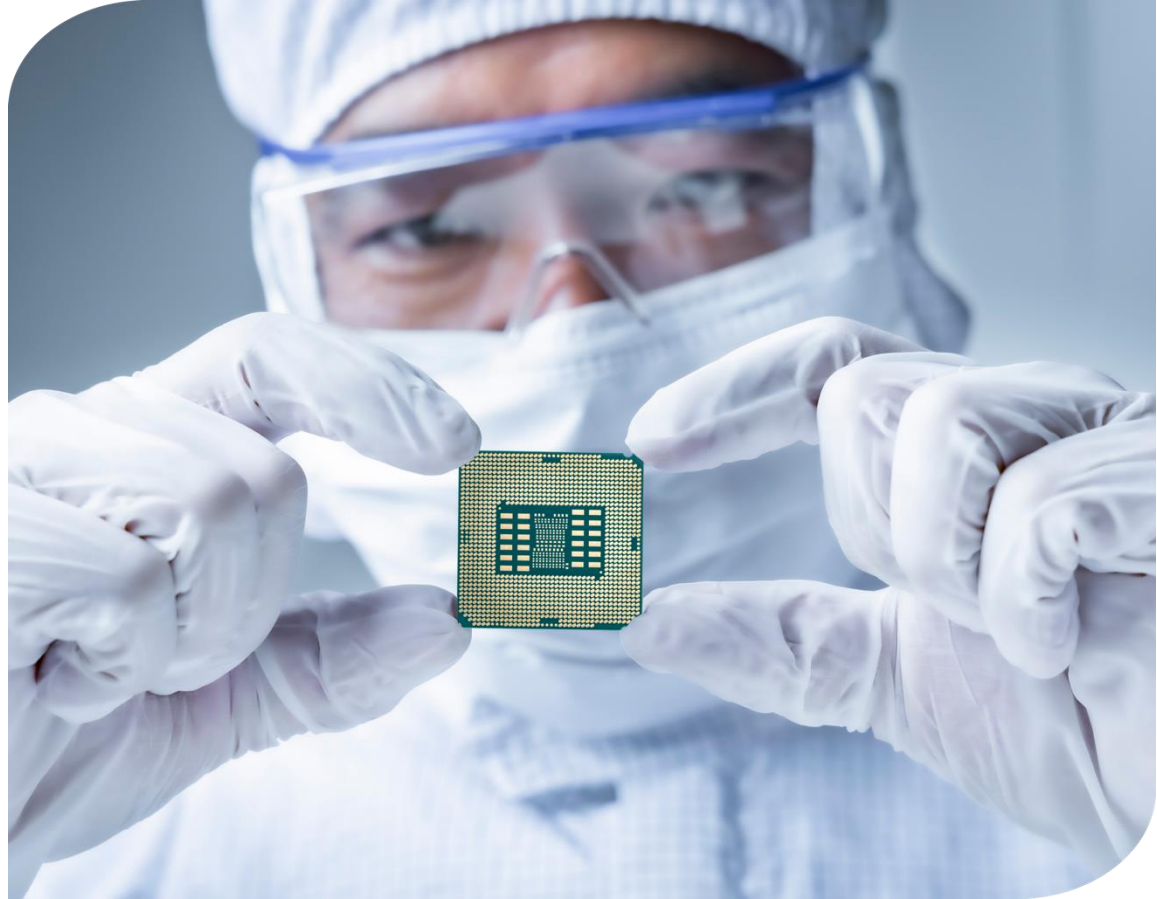
Dr. Peter Griehsnig
CTO

Responsible for:

- Environmental, Social and Governance
- Electronic Service Hub
- Information Security
- Corporate Quality
- Research & Development
- Technology & Innovation Management

Results

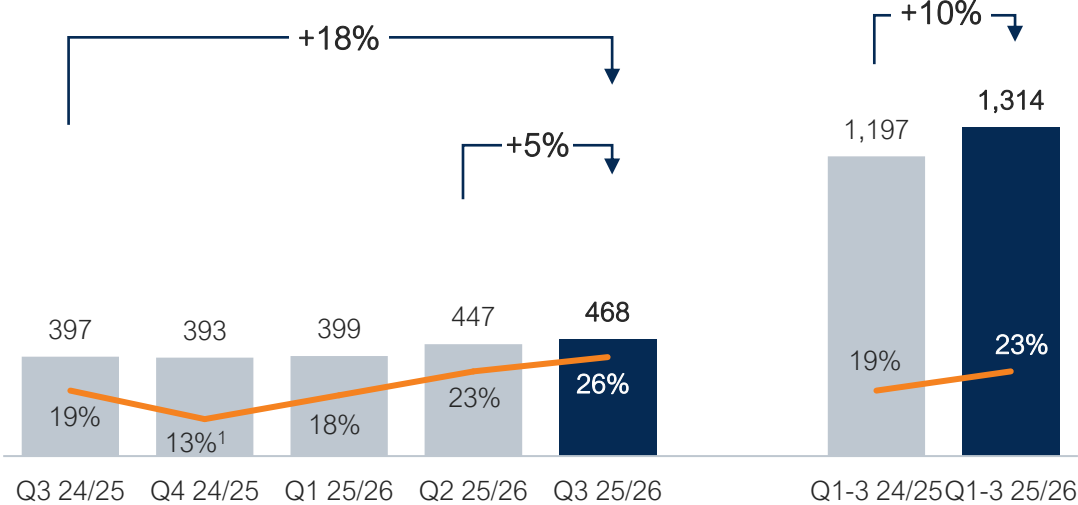
9M 2025/26



Q1-3 2025/26 results summary

Revenue and EBITDA margins

in € MM



■ 3rd party revenue — EBITDA margin

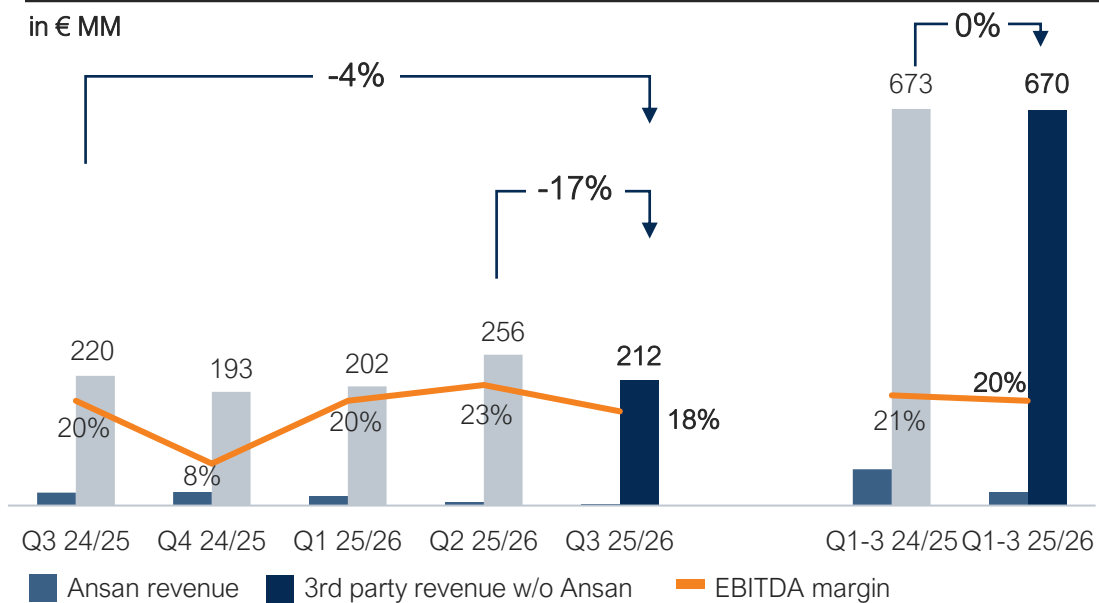
- **Q1-3 revenue:** ramps, positive product mix/volume and pricing effects compensated for reduced Ansan revenue as well as FX headwinds
- **Q1-3 margin:** higher due to improved pricing, product mix/volume as well as successful cost reduction despite FX headwinds and missing Ansan contribution

¹ Excludes proceeds from Ansan sale;
Margin incl. Ansan sale = 95%

Q1-3 2025/26 Business Unit: Electronics Solutions

Revenue and EBITDA margins

in € MM

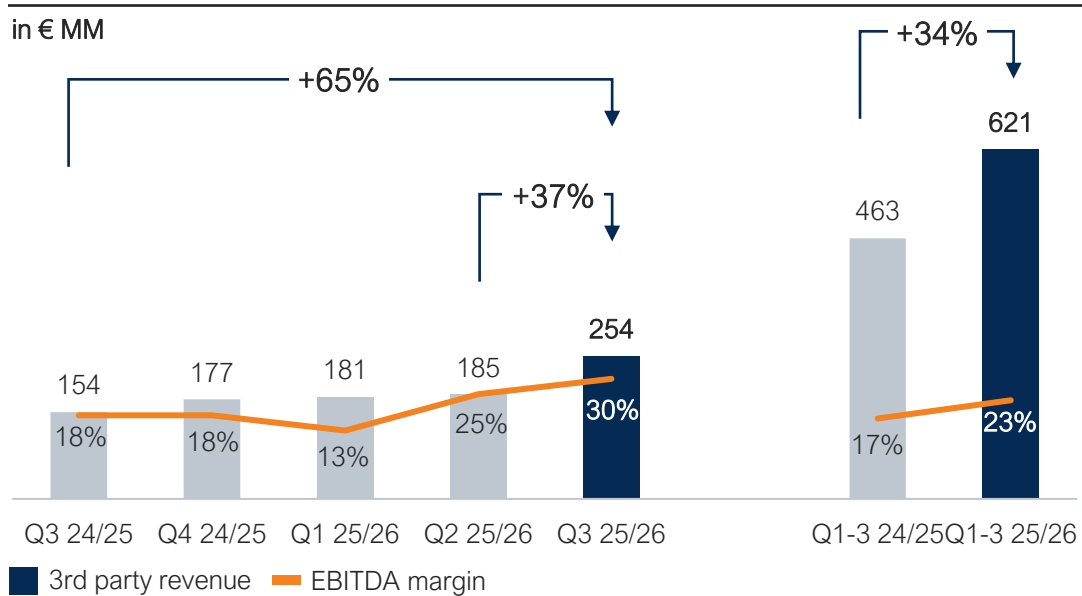


- **Q3 YoY decrease:** positive product mix/volume outweighed by missing Ansan revenue as well as pricing and FX headwinds
- **Q3 QoQ decline:** driven by seasonal effect of mobile devices

Q1-3 2025/26 Business Unit: Microelectronics

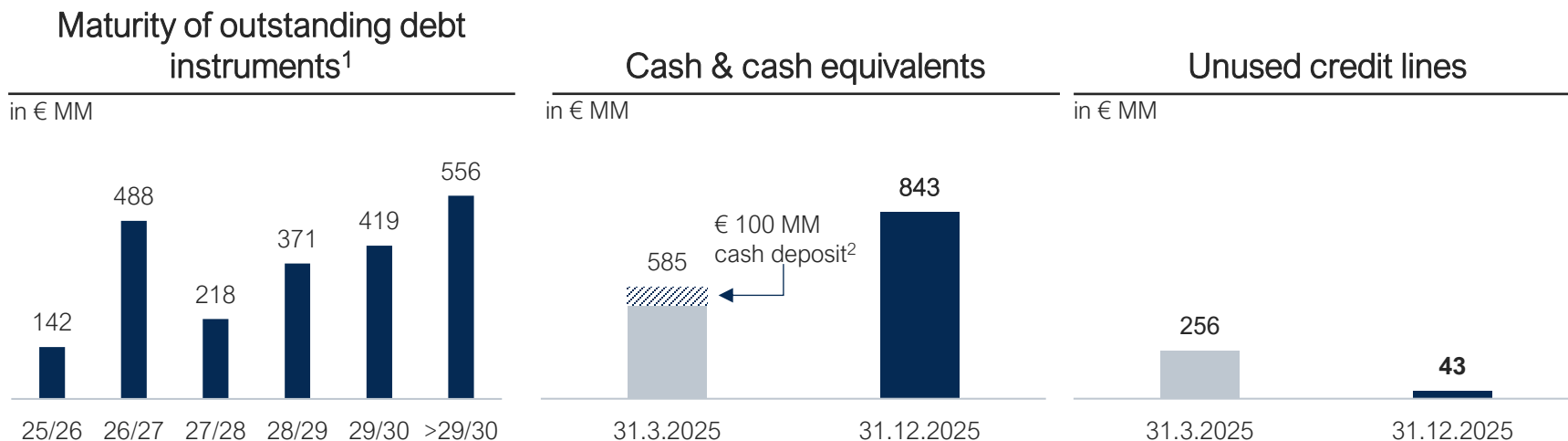
Revenue and EBITDA margins

in € MM



- **Q3 YoY growth:** Kulim and Leoben-Hinterberg ramp, supported by favorable volume/mix and pricing development
- **Q3 QoQ growth:** driven by ramps and positive mix as well as pricing effects
- **Result** benefits from customer agreements

Maturity profile & financial position



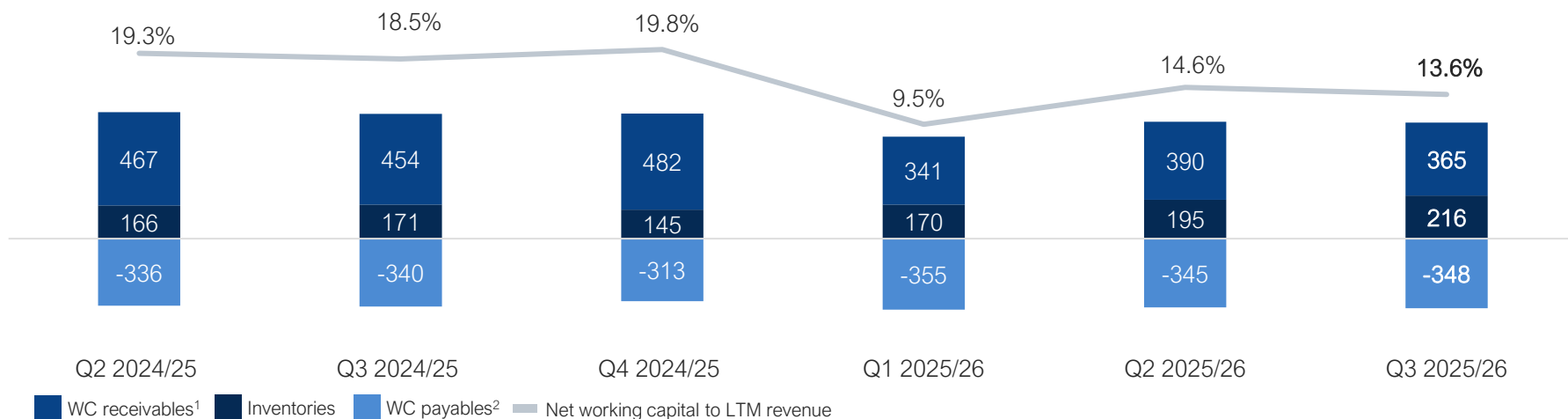
- Solid financial structure with **€ 886 MM** cash, cash equivalents and unused credit lines
- Current financing costs of **3.07%** (as of Q3 2025/26)

¹ Amounts by maturity as of December 31, 2025. Promissory note loans, term loans with banks, bank borrowings and others; including accrued interest and placement costs and finance leases | ² Due to maturity >90 days (due date May 5)

Working capital development

Working capital and relation to revenue

in € MM



¹ Trade and other receivables and contract assets

² Trade and other payables and other current provisions, without liabilities from investments

Cash flow

CAPEX reduction well on track

€ MM	Q1-3 24/25	Q1-3 25/26	YoY Change in %
CF from operating activities	-29	332	n.a.
CF from investing activities	-306	-26	+92%
CF from financing activities	192	83	-57%
Operating free CF ¹	-357	223	n.a.
Net CAPEX	-328	-108	-67%

- Strong EBITDA
- Factoring extended
- Cash deposits decreased
- Lower CAPEX

Balance sheet

Improved leverage

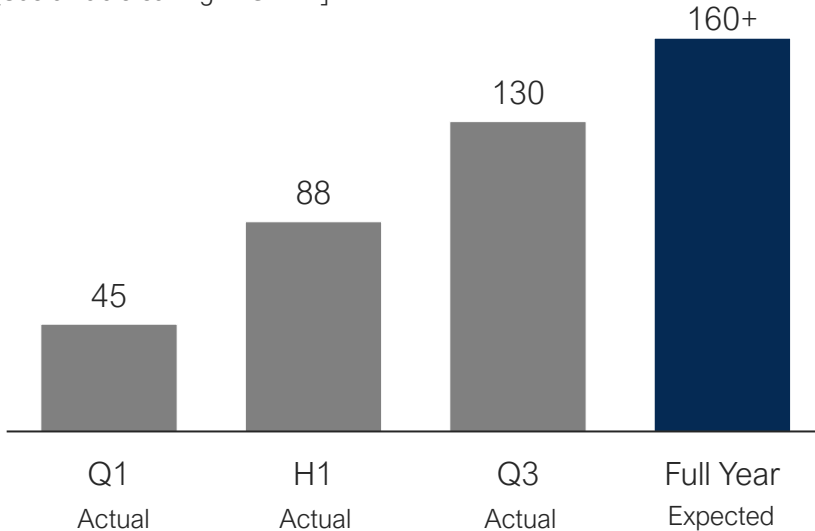
€ MM	March 31, 25	December 31, 25	Change in %	
Total assets	4,622	4,612	0%	• Including higher cash & cash equivalents
Equity	1,075	961	-11%	• Impacted by FX
Equity ratio	23.3%	20.8%	-2.4pp	
Net debt	1,491	1,316	-12%	• Net debt/EBITDA ratio: 2.0

Cost saving and efficiency program

Strong focus on sustainable OPEX savings

FY25/26 saving development, expected

[Sustainable saving in € MM]



Comment

- Full-year savings expected at least € 160 MM, exceeding the planned saving target of € 130 MM
- Savings driven by structural measures across Operations, Procurement, and SG&A

Kulim and HTB-ICS OPEX saving excluded from the program and managed separately, due to the ramping situation

2025/26 guidance

FY 2025/26e

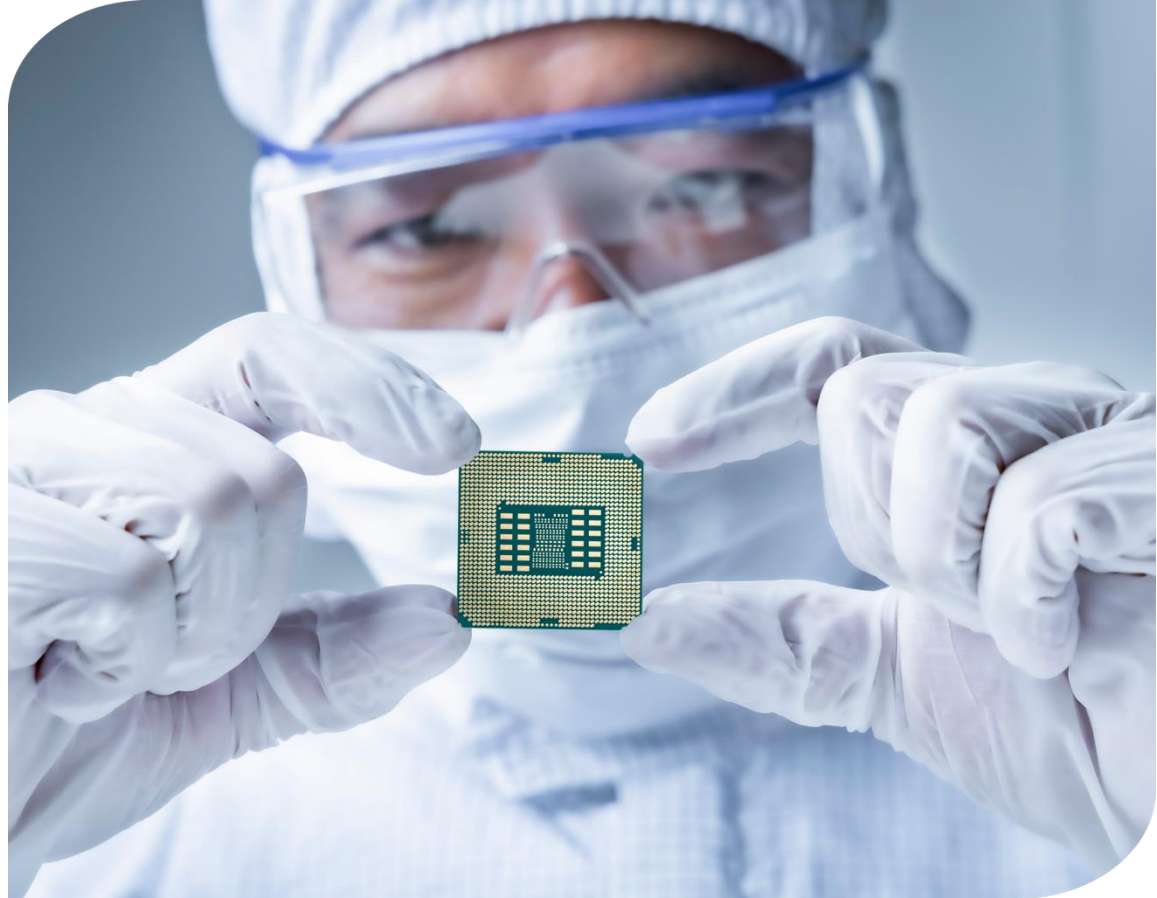
Revenue	Approx. € 1.7 BN
Profitability	EBITDA margin of approx. 23%
Investments	Net CAPEX approx. € 200 MM
Others	Maintain positive EBIT and Operating Free Cash Flow

2026/27 guidance

FY 2026/27e

Revenue	Approx. € 2.1 to 2.4 BN
Profitability	<ul style="list-style-type: none">• EBITDA margin of 24–28%• ROCE below the mid-term target of 12%
Others	<ul style="list-style-type: none">• Net debt/EBITDA: <3 (can be temporarily exceeded)• Equity ratio temporarily <20% (assuming repayment of hybrid capital at the end of the 2026/27 financial year)

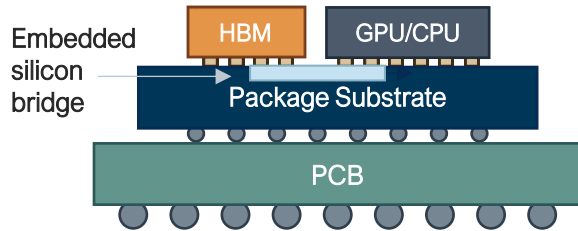
Technological trends



The role of Substrates and PCBs in Advanced Packaging

EMIB(-T)

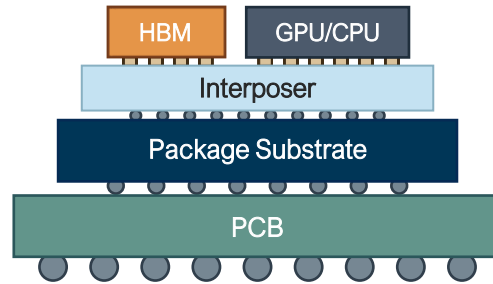
Embedded Multi-die Interconnect Bridge
(with Through-Silicon Vias)



- Cutting-edge substrate technology
- Moving complexity to the substrate
- Scales cost efficient with size

CoWoS

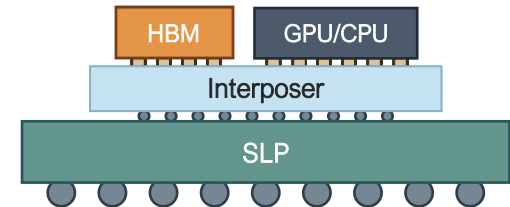
Chip-on-Wafer-on-Substrates



- Advanced substrate technology
- Complexity balanced between interposer & substrate
- Size scaling requires larger interposer

CoWoP

Chip-on-Wafer-on-PCB



- Essentially merging Substrate and PCB technology
- Several new technology to be industrialized
- Size scaling requires larger interposer

Enabling next generation power levels

Power stages at different locations enable unprecedented power levels

PMIC

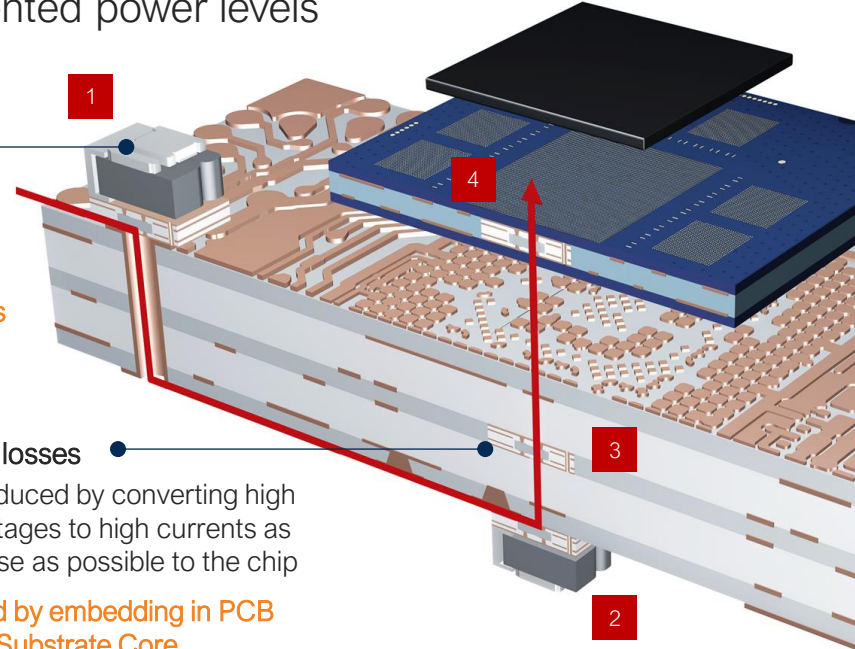
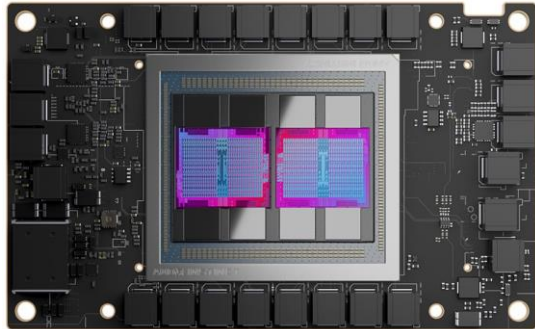


Conversion losses

→ Reduced by moving components closer

Enabled by embedding as a packaging technology for PMICs

MI350



Ohmic losses

→ Reduced by converting high voltages to high currents as close as possible to the chip

Enabled by embedding in PCB and IC Substrate Core

Q&A



Thank you for your attention

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